DAP 840 Manual

Installation Guide and
Connector Reference

Version 1.01

Microstar Laboratories, Inc.

Contents

1. Introduction

The Data Acquisition Processor from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 840 is a high-performance Data Acquisition Processor suitable for high-speed data acquisition and control.

Features of the DAP 840:
- TI486SXLC2-50 CPU
- PCI bus interface
- 14-bit A/D converter
- 50 ns TIME resolution
- 800K samples per second
- ±2.5 volt, ±5 volt, 0-5 volt, and ±10 volt analog input ranges
- ±2.5 volt, ±5 volt, 0-5 volt, 0-10 volt, and ±10 volt analog output ranges

The onboard operating system for the DAP 840 is DAPL 2000, which is optimized for 32 bit operation.

About This Manual

This manual includes hardware and software installation instructions, a hardware connector reference, hardware operation reference, and recalibration instructions. Two other manuals provide information about creating data acquisition applications:
- The DAPL Manual contains a complete DAPL reference.
- The Applications Manual contains many useful examples of Data Acquisition Processor applications.

2. Installation, Testing, & Troubleshooting

Installing a Data Acquisition Processor involves the following steps:

1. Install the Data Acquisition Processor.
2. Install the DAP Software.
3. Test the Installation.

Installation instructions are provided in this chapter. If there are any problems with installation, please read the troubleshooting guide at the end of this chapter.

Data Acquisition Processor Handling Precautions

Static control is required for handling all electronic equipment. The Data Acquisition Processor is especially sensitive to static discharge because it contains many high-speed analog and digital components. To protect the Data Acquisition Processor, observe the following precautions:

- Wear a grounding strap when handling the Data Acquisition Processor. If it is not possible to use a grounding strap, continuously touching a metal screw on a grounded PC offers protection.
- If it is necessary to transport the Data Acquisition Processor outside of the PC, be sure to shield the Data Acquisition Processor in a conductive plastic bag. If a conductive bag is not available, shield the Data Acquisition Processor by wrapping it completely in aluminum foil. Do not ship or store a Data Acquisition Processor in plastic peanuts without suitable shielding.

Static damage to analog components can cause subtle problems, including oscillation, increased settling time, and reduced slew rate. If you suspect that a Data Acquisition Processor has been affected by static discharge, return it to Microstar Laboratories for testing, repair, and quality control.

System Requirements

The DAP 840 is compatible with 5V 32 bit PCI Bus slots that support bus-mastering in 486/Pentium/Pentium Pro/Pentium II/Pentium III computers and requires Windows 95, Windows 98 or Windows NT 3.51 or later.

Installing the Data Acquisition Processor

Caution: Do not install the Data Acquisition Processor while the PC is on.

To Install the Data Acquisition Processor:

1. Turn off the PC and remove the PC's cover.
2. Insert the Data Acquisition Processor into any free PCI slot.
3. Screw down the back panel of the Data Acquisition Processor to the back chassis of the PC.

The Data Acquisition Processor requires approximately 15 Watts from the PC's power supply. If your system behaves erratically with the Data Acquisition Processor installed, the PC may need a larger power supply.

Installing Several Data Acquisition Processors

Many Data Acquisition Processor boards can operate simultaneously in one PC. Running several boards in parallel increases the maximum sampling rate and the real-time processing power of a system. The driver supports up to 14 Data Acquisition Processor boards in one PC. However, the number of Data Acquisition Processor boards is limited by the number of available PCI slots in the PC.

Installing DAP Software

When you insert the DAPtools CD into your CD-ROM drive, the Microstar Laboratories Setup Launcher will automatically run. When you select the 'Getting Started' link, you will obtain instructions for installing DAP software.

If the Windows hardware installer asks for the INF file, you can find the MSLACOM.INF file at the root of the DAPtools CD.

You can obtain more detailed instructions for installing DAP software under various operating systems by selecting the 'Documentation' link, followed by 'DAPtools Basic|Accel32|Installation'.

Testing Installation

To test the software installation, run the `DAPlog.EXE` program.

Troubleshooting

If the Accel32 Service will not start, check the host PC hardware manual to make sure that the particular PCI slot that the DAP uses supports bus-mastering. If necessary, switch to a different slot.

3. DAP 840 Connectors

This chapter discusses the interface connectors on the DAP 840. Diagrams and documentation for the analog input/output connector, the digital input/output connector, the output clock connector, and jumpers are provided in this chapter. Also included are detailed instructions for setting the following options:

• the analog input voltage range (J7, J8, J9, & J14)
• the output voltage ranges of DAC0 and DAC1 (J11 and J12)
• the digital output polarity at power-on (J32)
• input/output synchronization (J22)

Figure 1 shows component placement outlines of the DAP 840. The only components shown are connectors, whose labels begin with the letter J, some integrated circuits, whose labels begin with the letter U, and trim potentiometers, whose labels are single letters.
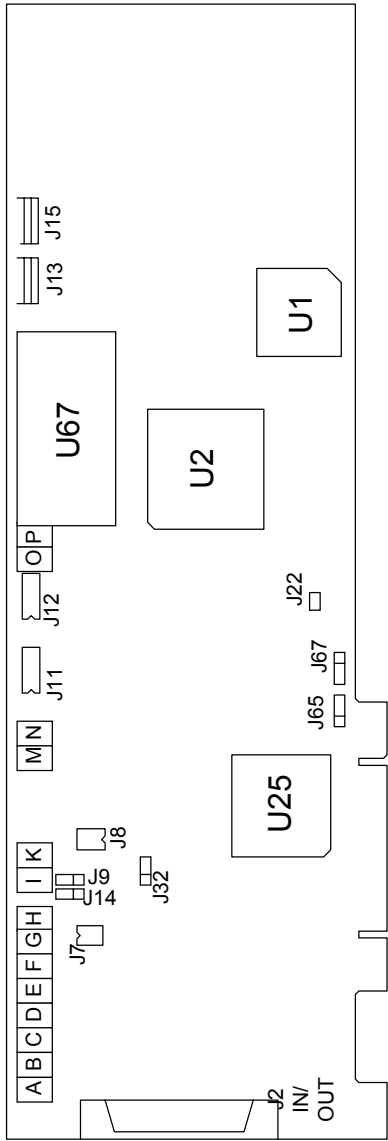
Figure 1.
DAP 840

Input/Output Connector

Analog and digital voltages are connected to the Data Acquisition Processor through a 50-pin connector on the back panel of the PC. This connector is located on the left side of the Data Acquisition Processor and is labeled J2 IN/OUT. It has a double row of pins on 0.050 inch centers. The connector is AMP part number 787394 5. This connector mates with discrete wire connector T&B part number HFM050A or insulation displacement connector AMP part number 786090 5. J2 mates with cable part numbers MSCBL 047-01, MSCBL 048-01, MSCBL 049-01K, MSCBL 050-01, and MSCBL 051-01K.

Looking at the input/output connector from the back of a PC, the pin numbering is:

DAP -18V	26 • • 25	DAP +18V
DAC 0 OUT	27 • • 24	DAC 0 GROUND
DAC 1 OUT	28 • • 23	DAC 1 GROUND
S7 (D3+)	29 • • 22	G7 (G3+)
S6 (D3-)	30 • • 21	G6 (G3-)
S5 (D2+)	31 • • 20	G5 (G2+)
S4 (D2-)	32 • • 19	G4 (G2-)
S3 (D1+)	33 • • 18	G3 (G1+)
S2 (D1-)	34 • • 17	G2 (G1-)
S1 (D0+)	35 • • 16	G1 (G0+)
S0 (D0-)	36 • • 15	G0 (G0-)
RESERVED	37 • • 14	ANALOG GROUND
EXTERNAL OUTPUT CLOCK - INPUT	38 • • 13	EXTERNAL INPUT CLOCK - INPUT
INTERNAL INPUT CLOCK - OUTPUT	39 • • 12	EXTERNAL TRIGGER
+5 VOLTS	40 • • 11	+5 VOLTS
DIGITAL GROUND	41 • • 10	DIGITAL GROUND
RESERVED	42 • • 9	RESERVED
DIN 0	43 • • 8	DOUT 0
DIN 1	44 • • 7	DOUT 1
DIN 2	45 • • 6	DOUT 2
DIN 3	46 • • 5	DOUT 3
DIN 4	47 • • 4	DOUT 4
DIN 5	48 • • 3	DOUT 5
DIN 6	49 • • 2	DOUT 6
DIN 7	50 • • 1	DOUT 7

Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended analog inputs are indicated by `S0` through `S7`; their corresponding ground inputs are `G0` through `G7`. Differential inputs are indicated by `D0-` and `D0+` through `D3-` and `D3+`; their corresponding ground inputs are `G0-` and `G0+` through `G3-` and `G3+`.

Digital inputs are indicated by `DIN 0-7` and digital outputs are indicated by `DOUT 0-7`. Bit 0 is the least significant bit.

Digital-to-analog outputs are indicated by `DAC0` and `DAC1`. Their corresponding ground returns are `DAC0 GROUND` and `DAC1 GROUND`.

Pin 13 is the external input clock input and pin 39 is the internal input clock output. Pin 12 is the external input trigger connection. Pin 38 is the external output clock input.

Pins 11 and 40 are connected to the 5-volt digital power supply. Pins 25 and 26 are +18-volt and 18-volt supplies respectively.

Pins 9, 37 and 42 are reserved and should not be used.

A termination board, the MSTB 010, described in Chapter 6, connects all lines of the input/output connector to discrete wire connectors.

The following sections describe the input/output connector pins in greater detail.

Analog Input

Analog voltages are connected to the DAP 840 through the 50-pin input/output connector on the back panel of the PC.   See the previous section for the input/output connector pinout.

A single-ended analog signal should be connected to an analog input pin and to the adjacent analog ground pin, for example to pins 36 and 15. A true differential analog signal should be connected to two adjacent analog input pins, for example to input pins 36 and 35. An additional connection must be made to ensure the common mode voltage is within the DAPs limits; otherwise, severe damage may result. One way to affect this is to tie a field ground reference to either of the associated ground pins. For example, the field ground could be tied to either ground pin 15 or ground pin 16. An alternative technique is to connect each ground pin to its corresponding signal pin through a resistor. This might be accomplished by tying a 1M Ohm resistor from the signal input on pin 35 to ground on pin 16, and another 1M Ohm resistor from the signal input on pin 36 to the ground on pin 15. In general, resistor values should be matched and selected to exceed the application's minimum input impedance requirements. Stiffer resistance values will help minimize crosstalk, a potential disadvantage of this technique.

Note: All analog ground pins are electrically connected on the DAP. If unrelated field grounds are tied to the DAP through the `G0..G7` (or through `G0-/G0+..G3-/G3+`) the grounds will become joined. If a floating ground system is connected in this manner, it will no longer be isolated from the DAP ground.

Analog input signals should be within the range from -10 volts to +10 volts, relative to the ground of the Data Acquisition Processor. The DAP 840 is provided with fault-protected input multiplexers. The analog inputs are protected against voltages up to ±40 volts. Input signals within this range may be applied to the DAP 840 when the PC's power is off.

Analog Output

The input/output connector on the DAP 840 includes digital-to-analog converter outputs. Pins 27 and 28 are the outputs of `DAC0` and `DAC1`, respectively. Pins 24 and 23 are the corresponding grounds. The digital-to-analog converters have voltage outputs with typical output impedances of 0.2 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on. When `J32` is moved, the analog outputs at power-on may vary by up to 5 millivolts.

Digital Input/Output

Digital input and output pins are located on the input/output connector on the back panel of the PC.

Digital inputs are indicated by `DIN 0-7` and digital outputs are indicated by `DOUT 0-7`. Bit 0 is the least significant bit.

The digital inputs are FCT TTL; they sink no more than 5 microamps for a "1" input and source no more than 0.43 milliamps for a "0" input. An input voltage greater than 2V is interpreted as a "1" and an input voltage less than 0.8V is interpreted as a "0". Each digital input has a 10K Ω pull-up resistor to +5 volts.

Digital inputs may have signals applied when the Data Acquisition Processor is off.

Digital outputs are set to "0" when the system is first powered on. The digital outputs are FCT TTL; they can sink no more than 12 milliamps for a "0" output and can source no more than 15 milliamps for a "1" output. The output voltage for a "1" is at least 2.4V and the output voltage for a "0" is at most 0.55V.

External Clock and Trigger

The input/output connector on the DAP 840 includes connections for internal clock output, external clock input, and external trigger input.

The external input clock—input pin is used to connect an external input clock to the DAP 840. The internal input clock—output pin is the buffered output of the DAP 840 input clock circuit.

Pin 12 is an external trigger connection. The external trigger for the DAP 840 is either one-shot or gated, depending on the `HTRIGGER` command in the active input procedure. The external trigger of the DAP 840 is ignored if there is no `HTRIGGER` command in the active input procedure.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off. See Chapter 5 for more information about the external clock and the trigger.

Supply Voltages

The input/output connector provides connections to DAP 840 supply voltages. Pins 25 and 26 are connected to +18 volt and -18 volt analog supplies. These supplies can be used for low current, low noise devices such as external multiplexers. The maximum allowable current drain from these supplies is 20 milliamps per side. If more current than this is required, either use an external supply or use the 5 volt digital power supply found on pins 11 and 40. The 5V supply has two connections on the Input/Output Connector; the output current is rated at 500 milliamps per connection.

Output Clock Connector

Connector `J15` is a five pin connector, Molex part number 22 23 2051; the mating connector is Molex part number 22 01 3057. `J15` is located on the top edge of the Data Acquisition Processor, near the right side of the board.

The output clock signals and the output trigger signal are on connector `J15`, along with power and ground. These signal pins can be used to control when outputs are updated. See Chapter 5 for more details.

The pin numbering for `J15` is given in the following table:

```
 1  2  3  4  5        Pin 1  Ground
 •  •  •  •  •         Pin 2  External output trigger - input
                      Pin 3  Internal output clock - output
                 J15  Pin 4  External output clock - input
                      Pin 5  +5 volts
```
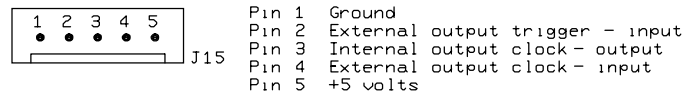
Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. instrumentation amplifier
3. programmable gain amplifier
4. range amplifier
5. analog-to-digital converter with sample-and-hold amplifier

Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the range amplifier, and also determine the input voltage range.

A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The range amplifier allows the bipolar analog-to-digital converter to operate with unipolar voltages. Jumpers select from three bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 500 are software selectable.

Analog Signal Path Configuration

Four connectors control the analog signal path of the DAP 840. Note that changing voltage ranges may require recalibration.

The following table summarizes the DAP 840 analog input jumper connections:

| ADC Range	J7	J8	J9	J14
0 to 5 v	2	3	1 - 2	1 - 2
± 2.5v	1	2	2 - 3	1 - 2
± 5v*	2 *	3 *	2 - 3 *	1 - 2 *
± 10 v	2	3	2 - 3	2 - 3

* Factory Configuration

The input signal to the range amplifier is selected by J7.

J7
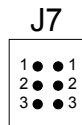
Exactly one jumper should be placed on J7, as follows:

Jumper	Range amplifier input
1	range amplifier disabled
2	programmable gain amplifier
3	instrumentation amplifier

The input signal to the analog-to-digital converter is selected by J8.

```
3 ●  ● 3
2 ●  ● 2
1 ●  ● 1
```
J8
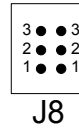
Exactly one jumper should be placed on J8, as follows:

Jumper	Analog-to-digital converter input
1	instrumentation amplifier
2	programmable gain amplifier
3	range amplifier

Note that jumpers on J7 and J8 are placed horizontally.
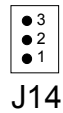
The signal range of the range amplifier is selected by J9 and J14. J9 selects between unipolar inputs and bipolar inputs.

```
● 3
● 2
● 1
```
J9
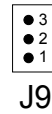
One jumper should be placed on J9 as follows:

Jumper	Signal range
1-2	unipolar
2-3	bipolar

J14 selects the input signal range of the range amplifier.

```
● 3
● 2
● 1
```
J14

One jumper should be placed on `J14` as follows:

Jumper	Input signal range
1-2	0 to 5 Volts
1-2	± 2.5 Volts
1-2	± 5 Volts
2-3	± 10 Volts

Note: Regardless of the input voltage range, positive and negative differential signals may range from -40 volts to +40 volts without damaging the Data Acquisition Processor .
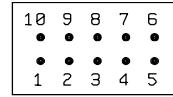
Note: There is a maximum speed reduction for the ±10-volt input range in order to get 14-bit accuracy on the DAP 840. Using the input voltage range of ±10 volts, the minimum `TIME` is 2.4 µs, which is approximately 417K samples/second.

Analog Output Voltage Range Selection

The voltage ranges of `DAC0` and `DAC1` are selected by headers `J11` and `J12`, respectively:
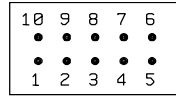
```
┌─────────────────┐          ┌─────────────────┐
│ 10  9  8  7  6  │          │ 10  9  8  7  6  │
│  •  •  •  •  •  │          │  •  •  •  •  •  │
│  •  •  •  •  •  │          │  •  •  •  •  •  │
│  1  2  3  4  5  │          │  1  2  3  4  5  │
└─────────────────┘          └─────────────────┘

        J11                          J12
```

Three or four jumpers should be placed on `J11` and `J12`, as follows:

Jumpers	Range
2-3, 8-9, 4-5, 6-7	0 to 5 Volts
2-3, 8-9, 6-7	0 to 10 Volts
1-2, 9-10, 4-5, 6-7	± 2.5 Volts
1-2, 9-10, 6-7	± 5 Volts
1-2, 9-10, 5-6	± 10 Volts

Note: By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued: `OPTION BPOUTPUT=OFF`

Digital Output Reset Polarity Jumper

The digital output reset polarity jumper `J32` has three pins spaced at 0.100". `J32` is located in the upper left section of the Data Acquisition Processor below trimmers I and K.

The digital output reset polarity jumper allows selection of the digital output polarity at power-on. If the shunt is installed on pins 1-2 (pin 1 is on the left) of `J32`, all digital outputs will be reset to 0 at power-on. If the shunt is installed on pins 2-3 of `J32`, all digital outputs will be preset to 1 at power-on. All Data Acquisition Processors are shipped from the factory with shunts installed on pins 1-2 of `J32`. The voltage of the analog outputs at reset may vary by up to 5 millivolts when the shunt on `J32` is moved.

Input/Output Synchronization Header

The input/output synchronization header `J22` has two pins spaced at 0.100". `J22` is located approximately one inch to the right of the right set of gold fingers on the Data Acquisition Processor. If a shunt is placed on `J22`, the input trigger is connected to the output update clock. This causes a hardware input trigger to occur when an output procedure initiates its first update. This is used to synchronize input sampling to output updates.

Synchronization Connector

The synchronization connector `J13` has a single row of five pins on 0.100 inch centers. `J13` is located along the top edge of the Data Acquisition Processor near the right side of the board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

Note: When synchronizing the DAP 840 with ISA bus models of Data Acquisition Processors, the DAP 840 must be configured as the slave unit. When synchronizing the DAP 840 with PCI bus models of Data Acquisition Processors, the DAP 840 can be configured as either master or slave.

4. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:
 • The DC input impedance is very high.
  • At high sampling rates, the signal source impedance should be low.
  • Minimum sampling times are specified for unity gain.
  • At gain 10, the fastest sampling rate is slower than the fastest sampling rate at gain 1.
  • At gain 100 and 500, the fastest sampling rate is substantially slower than the fastest sampling rate at gain 1.

Analog Input Circuits

Data Acquisition Processor analog input signals pass through two analog multiplexers and then to an op amp with a FET input. The DC input impedance is very high, typically far in excess of 10M Ohms. The AC input impedance is dominated by the capacitance of the multiplexers.

Figure 2 shows a useful equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to multiplexer outputs. When an input signal is connected to the FET amplifier, the signal source must supply sufficient current to charge the equivalent capacitance of the multiplexers before the analog-to-digital conversion can start.

Figure 2
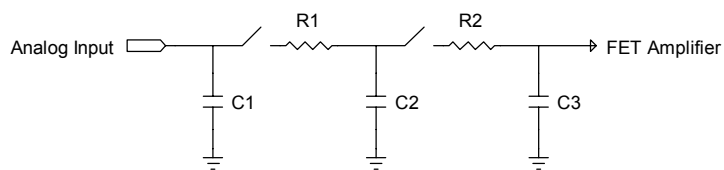
The DAP 840 has fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picofarads, for fault-protected multiplexers.

Component	Value
R1	400Ω
R2	400Ω
C1	5 pF
C2	30 pF
C3	25 pF

Programmable Gain Amplifier

At gains other than unity, the programmable gain amplifier requires extra time to switch from one channel to another and then settle to full accuracy. The following table shows typical minimum sampling times for the DAP 840 at each gain.

Minimum Sample Times in μS at Gain:

	1	10	100	500
DAP 840	1.25	8	40	500

5. Clocks and Triggers

The Data Acquisition Processor is designed to operate using either internal clocks or external clocks. The Data Acquisition Processor has onboard crystal-controlled timers to provide an internal input sampling rate and output update rate, and also has provisions for external clocks for both input and output.

The Data Acquisition Processor has hardware control lines for an input clock, an output clock, an input trigger, and an output trigger. These lines all are TTL compatible. The input clock and the output clock both are positive-edge triggered.

The input and output clocks of the DAP 840 have two modes. In the first mode, called Channel List Clocking, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single channel on the positive edge of the clock.

The input trigger and output trigger on all models also have two modes, a one-shot mode and a level-triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism which is suitable for most applications. For those applications which require precise synchronization to external hardware or which are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. Except in applications with high sampling rates combined with demanding processing requirements, software triggering almost always provides a better solution than hardware triggering.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the

trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be changed by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers, DAPL provides precise timing information. With hardware triggers, DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering does provide precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers.

Software and hardware triggers are implemented separately and may be used together.

External Input Clock

For most applications, there is no need to provide an input clock source to the Data Acquisition Processor; the on-board timer provides a wide range of sampling frequencies with fine time resolution. The main use of an external input clock is to precisely match the sampling rate to a standard frequency.

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least tSYNCH less than the period of the external clock. tSYNCH is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel list on the positive edge of the external clock. The second mode converts a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an input procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Example:

```
IDEF A 5
    CLOCK EXTERNAL
    CLCLOCKING ON
    SET IPIPE0 S0
    SET IPIPE1 S1
    SET IPIPE2 S2
    SET IPIPE3 S3
    SET IPIPE4 S4
    TIME 1000
    . . . .
    END
```

External input clocking is enabled for the input procedure A. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of channel 0 (S0) to channel 4 (S4). The channels are converted in sequence with channel 0 synchronized to the positive edge of the external clock and each of the subsequent channels converted according to the TIME command. Channel 1 (S1) is converted 1000 μs following the edge of the external clock, channel 2 (S2) is converted 2000 μs following the edge of the external clock, up to channel 4 (S4) which is converted 4000 μs following the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the TIME command times the number of channels plus tSYNCH. The external clock may be as slow as required—there is no maximum period.

If single channel clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one channel. The channels are converted in sequence. Each channel is synchronized to a positive edge of the external clock. In the previous application, channel 0 (S0) is converted on the first edge of the external clock, channel 1 (S1) is converted on the second edge of the external clock, and so on up to channel 4 (S4), which is converted on the fifth edge of the external clock. The channel list then is repeated with channel 0 converted again on the sixth positive edge of the external clock. When using single channel clocking, the period of the external clock (rising edge to rising edge) must be greater than the TIME command plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

Input Pipeline

The DAP 840 has one pipeline stage for analog and digital inputs. An input is acquired and read by the CPU on the same input clock cycle. Note that this is an

improvement over the DAP 3200a pipeline, where an input is acquired on one input clock cycle, and that acquired value is read by the CPU on the next input clock cycle.

The DAP 3200a and other ISA bus models of Data Acquisition Processors generate an additional input clock cycle when input sampling is stopped, in order for the CPU to read the last acquired value. When synchronizing multiple Data Acquisition Processors, the master generates the additional input clock cycle. The slave units depend on this additional clock cycle to read the last acquired value.

Because of its improved input pipeline, the DAP 840 does not generate an additional input clock when input sampling is stopped. Therefore, the DAP 840 must be configured as a slave unit when synchronizing the DAP 840 with other ISA bus models of Data Acquisition Processors.

The other PCI bus models of Data Acquisition Processors share the same single pipeline stage as the DAP 840. Therefore, the DAP 840 can be configured as either master or slave when synchronizing it with other PCI bus models of Data Acquisition Processors.

External Output Clock

For most applications, there is no need to provide an output clock source to the Data Acquisition Processor; the on-board timer provides a wide range of update frequencies with fine time resolution. The main use of an external output clock is to precisely match the output update rate to a standard frequency.

The external output clock on the Data Acquisition Processor is a positive-edge triggered TTL signal. Similar to the external input clock, the output clock is activated by the command `CLOCK EXTERNAL` in an output procedure. The `TIME` command of an output procedure with output clocking enabled must be at least tSYNCH shorter than the external clock period. tSYNCH and other times are defined at the end of this chapter. Unlike the external input clock, the first external output clock pulse is recognized.

On the DAP 840, external output clocking has two modes. The first mode, called Channel List Clocking, starts output of an entire channel list on the positive edge of the external clock. The second mode outputs a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an output procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued or the number of samples specified by the `COUNT` command of the input procedure is reached. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the input procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single channels, the input is stopped on channel boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a channel. When input sampling has been stopped with the gated trigger, synchronization of sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

Hardware Output Trigger

There are two modes for the output trigger of Data Acquisition Processors. The first mode is a one-shot mode and the second mode is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an output procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an output procedure is started. Output updating does not start until the trigger line is high. Updating continues until a `STOP` command is issued or the number of updates specified by the `COUNT` command of the output procedure is reached. The first updated value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the output procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, output updating may start and stop repeatedly, depending on the level of the trigger signal. The output is updated continuously when the trigger signal is high. Output updating stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When output clocking is configured in Channel List Clocking mode, the output is stopped only at channel list boundaries. When output clocking is configured to clock single channels, the output may stop after any channel. The effect of this is that the start of output is precisely synchronized to the positive edge of the trigger signal, assuming that output has stopped. Output stops when the Data Acquisition Processor has completed output of either a channel list or a channel. When output has been stopped with the gated trigger, synchronization of output to the positive edge of the trigger signal is the same as for the one-shot mode.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may only be determined if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT`, and `FIRFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling or output updating starts on a single event so all timing information is relative to the trigger event. In the case of a gated trigger, sampling or output updating may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

The Data Acquisition Processor acts upon the first external clock cycle after the trigger has been asserted, assuming input sampling has stopped. To guarantee recognition of an external trigger, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Using the Output Trigger with External Output Clocking

Output triggering may be used with external output clocking. To guarantee recognition of an external clock, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Timing tables

tSYNCH	200 ns	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input and output trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tTRIG_MAX	250 ns	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held
tOUTSKEW	30 ns	Time from output clock until start of DAC slewing

6. MSTB 010 DAP 800, DAP 820, DAP 840 Termination Board

The Microstar Laboratories Input/Output Termination Board, part number MSTB 010, is a 64-point quick-connect termination board for all connections on the DAP 840 input/output connector. The Input/Output Termination Board provides a ground connection for each input signal and each output signal, allowing easy connection to discrete devices.

All input connections are labeled with both the signal name and the pin number of the 50-pin connector on the Data Acquisition Processor. The pin numbers are discussed in Chapter 3.

Note: The Input/Output Termination Board should not be connected or disconnected while the Data Acquisition Processor is powered.

Analog Inputs

The analog inputs of the Input/Output Termination Board come from the factory configured for voltage input. The inputs can be configured for current input or for input voltages that exceed Data Acquisition Processor specifications.

The Input/Output Termination Board also can be used for differential analog inputs. A differential input is used to measure the difference between two voltages. The negative terminal voltage is subtracted from the positive terminal voltage. When a differential voltage is measured, a ground sense line must be connected between the Input/Output Termination Board and the signal source. Table 1 shows the correspondence between differential and single-ended inputs.

Table 1.

Single-Ended Input	Differential Input
S0	D0-
S1	D0+
S2	D1-
S3	D1+
S4	D2-
S5	D2+
S6	D3-
S7	D3+

Analog Outputs

The DAP 840 digital-to-analog converter outputs are available on the Input/Output Termination Board, along with a ground return for each output. The output current from each digital-to-analog converter output is rated at ± 5 milliamps, but it is recommended that this current not exceed ± 1 milliamp. The digital-to-analog converter outputs are voltage outputs.

Digital Input/Output

All digital input connections are labeled `DIx` where `x` is the input number; `x` ranges from 0 to 7. Each input connection has an adjacent ground connection. The inputs are directly connected to the DAP 840 so they have the same current limitations described for the DAP 840 in Chapter 3.

Digital input pins may have signals applied when the Data Acquisition Processor is off.

Note: If a voltage greater than 5V or less than 0V is applied to an input, damage to the Data Acquisition Processor may occur.

All digital output connections on the Digital Termination Board are labeled `DOx`, where `x` is the output number; `x` ranges from 0 to 7. Each output has an adjacent ground connection. The outputs are directly connected to the DAP 840 so they have the same current limitations described for the DAP 840 in Chapter 3.

All digital ground connections are electrically connected on the Input/Output Termination Board, and are connected to the Data Acquisition Processor ground. All digital signals connected to an Input/Output Termination Board must share the PC's ground as a common reference.

Note: If the digital output current is extended beyond maximum ratings, damage to the Data Acquisition Processor is possible.

Control Lines

The Input/Output Termination Board has connections to DAP 840 clock and trigger lines. The connection labeled `XC0` is the external input clock input. The buffered internal input clock output is labeled `INC`. The connection labeled `XC1` is the external output clock input. The external trigger input connection is labeled `TRIG`.

Power Supplies

The Data Acquisition Processor has unregulated ± 18 volt supply voltages; these are available on the Input/Output Termination Board. The maximum allowable current drain from these supplies is 20 milliamps per side. If more current than this is required, an external power supply should be used instead of the Data Acquisition Processor's ± 18 volt supply. The Input/Output Termination Board also has connections for the Data Acquisition Processor +5V power supply. The 5V supply has two connections on the Input/Output Termination Board; the output current is rated at 500 milliamps per connection.

Hardware Configuration

The Input/Output Termination Board is connected to a DAP 840 using a 50-line ribbon cable, part number MSCBL 050-01, or a 50-line round shielded cable, part number MSCBL 048-01. MSCBL 050-01 or MSCBL 048-01 connects the input/output connector of a DAP 840 to connector `J1` of the Input/Output Termination Board.

Current Input

To configure a current input, place a resistor in the location on the termination board corresponding to the input pin being reconfigured. Figure 5 and Table 2 show resistor placement. The appropriate size for this resistor can be calculated using Ohms law, given the maximum input current and the input voltage range of the Data Acquisition Processor.

```
Ohm's Law: Resistance = Voltage / Current
```

The Data Acquisition Processor is shipped from the factory with an input range of +/- 5 volts. The accuracy of the measurements made in this configuration depends on the precision of the resistors used and this should be taken into consideration when selecting the resistors. Microstar Laboratories recommends using resistors with a 1% or better tolerance.

Excess power dissipated in the resistor causes heating; this changes the resistance value, decreasing the accuracy of the measurements. The recommended maximum power dissipation is 0.1 watt.

```
Power Calculation: Power = current² * resistance
```

For current input, a current source is connected to the Sx terminal and the ground return is connected to the Gx terminal. To convert voltage input $S0$ into a current input that generates 1 to 5 volts with an input current of 4 to 20 milliamps, a 250 ohm resistor is inserted in the $R2$ location. In this case, the maximum power dissipated in the resistor is 0.1 watt at +5 volts; this is the maximum recommended power dissipation. Figure 3 illustrates the connections for this example.
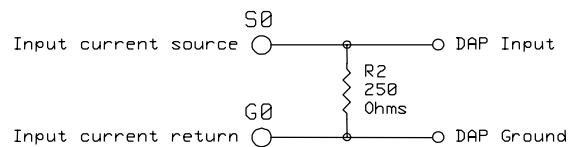
Figure 3.

Voltage Divider

The termination board can be configured for applications requiring input voltages greater than that allowed by the Data Acquisition Processor. This is accomplished by soldering a resistive voltage divider in the location provided on the termination board. Before this can be done, a trace on the termination board must be cut. Above each odd numbered resistor there is a row of five small holes. Between two of the holes there is a white "X". The trace at the X must be cut.

Once this trace is cut, the resistors for the voltage divider are soldered into place. The resistor on the ground side of the divider is placed in an even numbered resistor location and the resistor on the input signal side of the divider is placed in an odd numbered resistor location. Figure 5 and Table 2 illustrate resistor placement for each input.

After both resistors are soldered into place, signals may be connected between the Sx and Gx terminals. Test the voltage divider circuit before connecting the circuit to the Data Acquisition Processor.

Note: Be careful to avoid applying an input voltage that exceeds Data Acquisition Processor specifications.

Warning: If the trace on the termination board is not cut, the high voltage input is connected directly to the Data Acquisition Processor input; this may damage or even destroy the Data Acquisition Processor.

For example, to configure input S0 so that an input range of 0 to 20 volts is scaled down to a range of 0 to 5 volts, a resistor ratio of 3:1 is needed.

Voltage Divider Equation: $V_{out} = V_{in} * R1/(R1+R2)$

Resistance values of 1500 and 500 ohms may be used. The trace beneath the X above R1 is cut. Then the 500 ohm resistor is placed in the R2 position and the 1500 ohm resistor is placed in the R1 position. Since 500 ohm resistors are not commonly available, a 510 ohm resistor would typically be used instead, resulting in a small error in the division ratio. This error is linear and can be corrected by multiplying by a constant in DAPL. Figure 4 illustrates the circuit for this example.
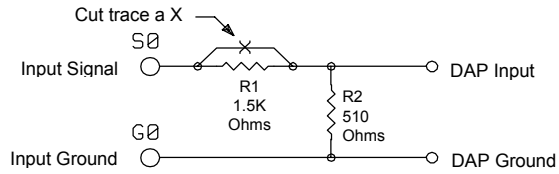
Figure 4.
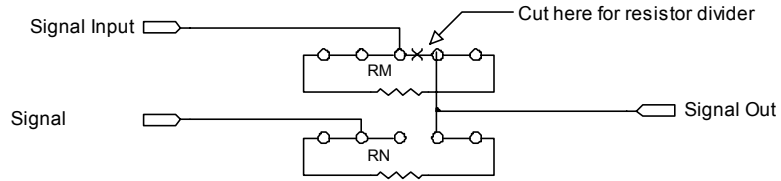
Figure 5.

Note: To avoid exceeding Data Acquisition Processor input voltage specifications, make sure both resistors are securely soldered in the correct locations and the trace beneath the X is completely cut before using the circuit.

Table 2.

Terminal	Current Input Resistor *	Voltage Divider Resistors
S0, G0	R2	R2, R1
S1, G1	R4	R4, R3
S2, G2	R6	R6, R5
S3, G3	R8	R8, R7
S4, G4	R10	R10, R9
S5, G5	R12	R12, R11
S6, G6	R14	R14, R13
S7, G7	R16	R16, R15

*   The current input resistor is placed in the RN location shown in the previous figure.

**   The first resistor is on the ground side of the voltage divider (RN), the second is on the input signal side (RM), as shown in the previous diagram. For example, R2 is RN and R1 is RM. Figure 5 shows the resistor placement.

Table 2 and Figure 5 can be used to locate the appropriate resistors when using either the current input or voltage division configuration. Figure 5 shows schematically how the inputs and grounds on the termination board are connected.

Cold Junction Reference

The Input/Output Termination Board has a cold junction reference circuit. This circuit is used to measure the temperature of the "cold junction" at the termination board. Since the cold junction temperature is the same for all thermocouples connected to a termination board, only one cold junction reference circuit is needed for any number of thermocouples.

The cold junction reference circuit generates a voltage which is temperature dependent. When jumper J5 is installed the output of this circuit are connected to single-ended input S7 of the termination board. The Data Acquisition Processor samples this voltage and the resultant information is used in the THERMO command for cold junction compensation. When the cold junction reference circuit and jumper J5 are installed, no other inputs should be connected to the S7 terminal, as it is connected to the cold junction reference circuit. Removing jumper J5 will disconnect the cold junction reference circuit from the S7 terminal.

The cold junction reference circuit is implemented with a Linear Technology LT1025 integrated circuit. This part provides a 10 mV/°C voltage output. The output voltage can be modeled by the following formula.

```
V₀ = 10mV/°C(T) + (10mV/°C)(5.5x10E-4)(T-25°C)²
```

The LT1025 has a nearly linear voltage output. For temperatures near room temperature, the quadratic error term is negligible and the voltage output is:

```
V₀ = 10mv/°C * T
```

See the Applications Manual for an example using the cold junction reference circuit.

7. Recalibration

Each Data Acquisition Processor is burned in and then calibrated by Microstar Laboratories. The accuracy of this calibration is sufficient for most applications. Accuracy is affected by three factors:
- the operating temperature of the Data Acquisition Processor
- drift in the Data Acquisition Processor circuitry
- analog voltage range selection.

The operating temperature is determined by a number of factors. If the Data Acquisition Processor is operated inside a personal computer, the operating temperature is affected by the number of expansion boards, power supply rating, fan efficiency, etc.

Component drift depends on total operating time of the unit as well as the number of times the unit has been powered up and down.

Changes to analog voltage ranges may require that the Data Acquisition Processor be recalibrated.

For applications requiring high accuracy, occasional recalibration may be necessary. For high absolute accuracy, the Microstar Laboratories calibration sequence requires that measurements be made using a 4.5 digit digital voltmeter with a DC accuracy of .024% (244 ppm) or better. In most applications, only relative accuracy is important, so recalibration with a less accurate digital voltmeter may be acceptable. Calibration also requires a variable voltage source with high stability.

Because calibration requires significant setup time, it generally is best to send Data Acquisition Processors to Microstar Laboratories for recalibration. Calibration is available from Microstar Laboratories for a nominal fee.

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