DAP 5400a Manual

Connector and Hardware Operation Reference

Version 1.01

Microstar Laboratories, Inc.

Microstar Laboratories, Inc.
2265 116th Avenue N.E.
Bellevue, WA 98004
Tel: (425) 453-2345
Fax: (425) 453-3199
www.mstarlabs.com

Part Number DAP5400AM101

Contents

1. Introduction

The Data Acquisition Processor from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 5400a is a high-performance Data Acquisition Processor suitable for high-speed data acquisition and control. The DAP 5400a uses eight analog-to-digital converters. Each analog-to-digital converter is connected to two single-ended input pins through a multiplexer. Each analog-to-digital converter is capable of sampling 1.25 million samples per second, making a maximum aggregate sample rate of 10 million samples per second. In a normal operating configuration, simultaneous sampling of the input pins occurs in groups of eight. For compatibility with earlier Data Acquisition Processors, the DAP 5400a can be configured to sample in groups of four.

Features of the DAP 5400a:

- AMD K6-III+ 400 MHz CPU
- 128 Megabytes SDRAM
- PCI bus interface
- Eight 14-bit A/D converters
- 20 ns TIME resolution
- 1.25M samples per second per channel
- 10M samples per second aggregate
- Inherent simultaneous sampling of 8 input pins
- No output and no digital port
- ±5 volt and ±10 Volt analog input ranges

The DAPL system assigns special names, called channel group members, for identifying the sets of signals that the DAP 5400a samples simultaneously. While channel groups can be configured to sample in any order, the channels within a group are fixed and the order of the channels in each group is pre-determined.

The onboard operating system for the DAP 5400a is DAPL 2000, which is optimized for 32 bit operation.

About This Manual

This manual includes a hardware connector reference, hardware operation reference, and recalibration instructions. The manual covers:

- Connectors, both for hardware configuration and for attaching control signals.
- The electrical characteristics of the input sampling circuit.
- Identification of the input sampling channels in the system configuration.
- Special features for hardware-controlled and software-controlled triggering to begin sampling.
- Configuring the Data Acquisition Processor to capture and process data streams.

Four other manuals provide installation instructions and information about creating data acquisition applications:

- The DAP PCI Installation Manual contains hardware and software installation instructions.
- The DAPL Manual contains a complete DAPL reference.
- The Applications Manual contains many useful examples of Data Acquisition Processor applications.
- The DAPstudio Manual explains how to configure applications.

The DAP 5400a is compatible with 5 Volt, 32 bit PCI Bus slots that support bus-mastering. Most PC hosts that support the Intel family of processors or compatible processors, and that are compatible with various versions of the Windows operating system from Windows 95 or later, will support Data Acquisition Processors.

2. DAP 5400a Connectors

This chapter discusses the interface connectors on the DAP 5400a. Diagrams and documentation for the analog input connector and synchronization connector are provided in this chapter.

Figure 1 shows component placement outlines of the DAP 5400a. The only components shown are connectors, whose labels begin with the letter J and some integrated circuits, whose labels begin with the letter U.

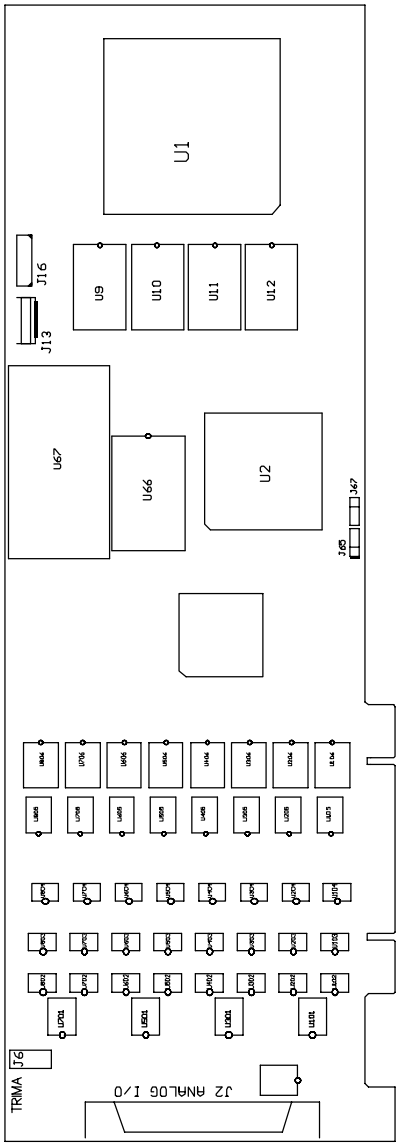


Figure 1.
DAP 5400a

Analog Input Connector

Analog voltages are connected to the Data Acquisition Processor through a 68-pin connector on the back panel of the PC. This connector is located on the left side of the Data Acquisition Processor and is labeled J2 ANALOG I/O. It has a double row of pins on 0.050 inch centers. This connector is 3M part number 10268-52E2VC or AMP part number 2-178238-8. It mates with discrete wire connector 3M part number 10168-6000EC or AMP 2-175677-8. Both connectors are shielded and are compatible with round cable. The analog I/O connector also mates with insulation displacement ribbon cable connector 3M part number 10168-8100EE. The insulation displacement connector is compatible with 0.025" pitch ribbon cable.

Looking at the analog connector from the back of a PC, the pin numbering is:

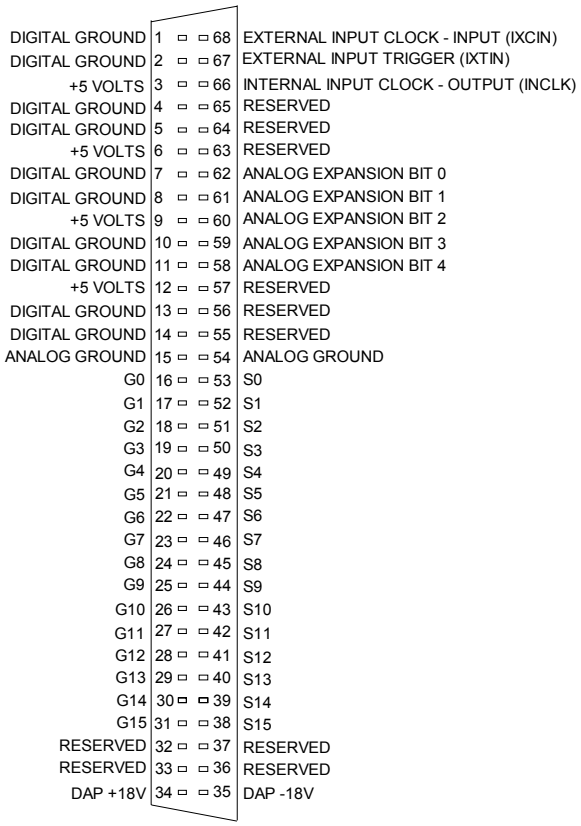


Figure 2. Analog Input Connector

Note: Use the pin numbering on this chart, rather than numbers that may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended inputs are indicated by `S0` through `S15`; their corresponding ground inputs are `G0` through `G15`. A single-ended analog signal and its ground should be connected to an analog input pin and an analog ground pin, for example to pins 53 and 16.

Termination boards that connect all lines of the analog connector to discrete wires are available from Microstar Laboratories.

The DAP 5400a features fault-protected input multiplexers. Fault protected input multiplexers allow signals to be connected to the Data Acquisition Processor with power off and allow a higher input voltage without damaging the inputs. Spare fault-protected input multiplexers are available from Microstar Laboratories.

Analog input signals should be within the range from -25 volts to +25 volts, relative to the ground of the Data Acquisition Processor. Input signals may be applied to the Data Acquisition Processor when the PC's power is off. See Chapter 5 for electrical characteristics of the analog input pins.

Pin 15 of the analog input connector is analog power ground. Pins 34 and 35 are connected to +18 volt and -18 volt analog supplies. The maximum allowable current drain from these supplies is 50 milliamps per side. These supplies can be used for low current, low noise devices such as external multiplexers. To supply power to other devices, either use an external supply or use the 5 volt digital power supply found on the analog control connector with an external DC-to-DC converter.

The analog input connector also provides analog input expansion control lines, an external trigger input, an external input clock input, an internal input clock output, and connections to the 5-volt digital power supply and its ground.

Pins 58 through 62 provide TTL-compatible analog input expansion control signals that select the expansion port. The five highest order bits of the input pin number appear in descending order on pins 58, 59, 60, 61, and 62 for a period starting one sample time before the analog input is sampled.

External analog input expansion boards are available from Microstar Laboratories. Each input expansion board allows up to 64 single-ended inputs. A Data Acquisition Processor can control up to 8 external expansion boards, for a total of 512 input lines.

The analog input connector has an input pin for an active high external trigger. The external trigger is either one-shot or gated, depending on the HTRIGGER command in the active input procedure. The external trigger is ignored if there is no HTRIGGER command in the active input procedure. See Chapter 6 for more information.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

The analog input connector has input and output pins for the input clock. The input pin is used to connect an external input clock. The output pin is the buffered output of the internal clock circuit. See Chapter 6 for more information.

Pins 3, 6, 9, and 12 provide +5 volt power. Maximum current from the +5 volt supply is 1 Amp.

Analog Signal Path

All analog signal path parameters are set with DAPL configuration options. The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. Input multiplexers
2. Buffer amplifier
3. Range amplifier
4. Analog-to-digital converter with sample-and-hold amplifier

Analog signals pass through all of these functional units. DAPL configuration options determine the input range for all eight analog input sections; all eight input sections have the same input range. Note that changing voltage ranges may require recalibration.

The input voltage range is selected by the DAPL command VRANGE in an input procedure. Voltage ranges of +/-5V and +/-10V are supported on the DAP 5400a. All channels use the same input voltage range. Because the VRANGE command establishes a default condition that is used for configuring all data channels, the VRANGE command should appear as one of the first commands following the IDEFINE command. To select the +/-5V range use VRANGE -5 +5 and to select the +/-10V range use VRANGE -10 +10.

A signal is single-ended if it is measured relative to ground. A signal is differential if it is measured relative to another signal. The DAP 5400a accepts only single-ended inputs; there are no provisions for differential inputs.

Note: There is a maximum speed reduction for the ±10-volt input range in order to get 14-bit accuracy on the DAP 5400a. Using the input voltage range of ±10 volts with a channel list that includes more than one channel group, the minimum `TIME` is 2.4 µs, which is approximately 417K samples/second.

Synchronization Connector

The synchronization connector `J13` has a single row of five pins on 0.100 inch centers. `J13` is located along the top edge of the Data Acquisition Processor near the right side of the board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 101-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

Note: When synchronizing the DAP 5400a with slower models of Data Acquisition Processors, the DAP 5400a may be the master only if it acquires no faster than the slower DAP can sample.

3. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:

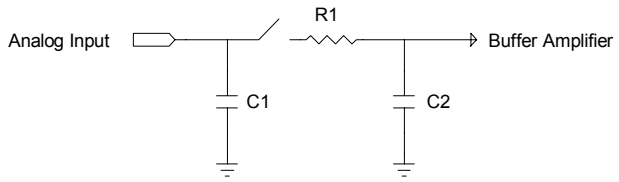
- The DC input impedance is high: 35 MegOhms minimum, 80 MegOhms typical.
- At high sampling rates, the signal source impedance should be low.
- Minimum sampling times are specified for +/-5V range and without switching the multiplexers.
- Signal source impedance and cable length significantly impact accuracy at high sample rates; short cables and low-impedance sources should be used.
- All inputs are single-ended with voltage ranges of +/-5V and +/-10V.

Analog Input Circuits

Data Acquisition Processor analog input signals pass through an analog multiplexer then to an op amp. The DC input impedance is high, typically 80M Ohms at DC. The AC input impedance is dominated by the capacitance of the multiplexer.

Figure 2 shows an equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to amplifiers. The signal source must be fast enough to charge the capacitance of the multiplexers in the time between analog-to-digital conversions otherwise accuracy will be reduced. Long cables increase the input capacitance while at the same time increasing the signal source impedance, thereby increasing the settling time of the input section.

Figure 3



The DAP 5400a has fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picoFarads, for fault-protected multiplexers.

Component	Value
R1	300Ω
C1	5 pF
C2	30 pF

Channel Groups

The DAP 5400a uses a different input configuration than other Data Acquisition Processors. It always samples input pins in groups. DAPL commands use a special notation to refer to these groups.

The DAP 5400a can sample either in groups of four or in groups of eight. To sample groups of eight channels simultaneously, specify in the input configuration:

```
GROUPSIZE 8
```

A four-channel mode is used mostly for compatibility with older products. To sample in groups of 4 channels simultaneously, specify in the input configuration:

```
GROUPSIZE 4
```

When defining a sampling configuration, the signals to sample are selected by a pin group name. The pin groupings for signals sampled simultaneously are predefined. The physical pins for each group name are listed in the tables below:

DAP 5400a 8-Channel Groups

Pin Group	DAP 5400a Pin
SPG0	S0, S2, S4, S6, S8, S10, S12, S14
SPG1	S1, S3, S5, S7, S9, S11, S13, S15

DAP 5400a 4-Channel Groups

Pin Group	DAP 5400a Pin
SPG0	S0, S2, S4, S6
SPG1	S1, S3, S5, S7
SPG2	S8, S10, S12, S14
SPG3	S9, S11, S13, S15

The pin numbers in these tables correspond directly to the physical pins on the analog input connector of DAP 5400a as shown in the figure 2 on page 5.

When using input expansion, the signals appear at different channel numbers on the termination boards. You can find complete information in Appendix A about where the signals connect.

4. Clocks and Triggers

The Data Acquisition Processor is designed to operate using either internal clocks or external clocks. The Data Acquisition Processor has onboard crystal-controlled timers to provide an internal input sampling rate and also has provisions for an external clock for input sampling.

The Data Acquisition Processor has hardware control lines for an input clock and an input trigger. These lines are TTL compatible. The input clock is positive-edge triggered.

The input clock of the DAP 5400a has two modes. In the first mode, called Channel List Clocking, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single channel on the positive edge of the clock.

The input trigger also has two modes, a one-shot mode and a level-triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism which is suitable for most applications. For those applications which require precise synchronization to external hardware or which are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. Except in applications with high sampling rates combined with demanding processing requirements, software triggering almost always provides a better solution than hardware triggering. Even at the maximum sample rate the DAP 5400a has enough processing power to perform software triggering looking for simple level crossing events. At lower sample rates the DAP 5400a can scan for extremely complicated events.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be modified by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers, DAPL provides precise timing information. With hardware triggers, DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering provides precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers and works equally well at all sample rates.

Software and hardware triggers are implemented separately and may be used together.

External Input Clock

For most applications, there is no need to provide an input clock source to the Data Acquisition Processor; the on-board timer provides a wide range of sampling frequencies with fine time resolution. The main use of an external input clock is to precisely match the sampling rate to a standard frequency.

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least tSYNCH less than the period of the external clock. tSYNCH is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel list on the positive edge of the external clock. The second mode converts a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an input procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Example:

```
IDEF A 2
     CLOCK EXTERNAL
     CLCLOCKING ON
     SET IPIPES(0..7) SPG0
     SET IPIPES(8..15) SPG1
     TIME 1000
     . . . .
END
```

External input clocking is enabled for the input procedure `A`. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of pin group 0 (`SPG0`) and pin group 1 (`SPG1`). The pin groups are converted in sequence with pin group 0 synchronized to the positive edge of the external clock and each of the subsequent pin groups converted according to the `TIME` command. Pin group 0 (SPG0) is converted at the rising edge of the external clock and pin group 1 (`SPG1`) is converted 1000 µs after the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command times the number of channels plus tSYNCH. The external clock may be as slow as required—there is no maximum period.

If single channel clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one pin group. The pin groups are converted in sequence. Each pin group is synchronized to a positive edge of the external clock. If single channel clocking were used in the previous application, pin group 0 (`SPG0`) would be converted on the first edge of the external clock and pin group 1 (`SPG1`) would be converted on the second edge of the external clock. The channel list then is repeated with channel 0 converted again on the third positive edge of the external clock. When using single channel clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

Input Pipeline

The DAP 5400a has one pipeline stage for analog inputs. An input is acquired and read by the CPU on the same input clock cycle.

The DAP 3200a and other ISA bus models of Data Acquisition Processors generate an additional input clock cycle when input sampling is stopped, in order for the CPU to read the last acquired value. When synchronizing multiple Data Acquisition

Processors, the master generates the additional input clock cycle. The slave units depend on this additional clock cycle to read the last acquired value.

Because of its improved input pipeline, the DAP 5400a does not generate an additional input clock when input sampling is stopped. Therefore, the DAP 5400a must be configured as a slave unit when synchronizing the DAP 5400a with other ISA bus models of Data Acquisition Processors.

The other PCI bus models of Data Acquisition Processors share the same single pipeline stage as the DAP 5400a. Therefore, the DAP 5400a can be configured as either master or slave when synchronizing it with other PCI bus models of Data Acquisition Processors.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued or the number of samples specified by the `COUNT` command of the input procedure is reached. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the input procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low. The active period of the input trigger must be less than tTRIG_MAX to guarantee acquisition of only one sample.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single channels, the input is stopped on channel boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a channel. When input sampling has been stopped with the gated trigger, synchronization of

sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may only be determined if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT`, and `FIRFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling starts on a single event so all timing information is relative to the trigger event. In the case of a gated trigger, sampling may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

The Data Acquisition Processor acts upon the first external clock cycle after the trigger has been asserted, assuming input sampling has stopped. To guarantee recognition of an external trigger, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Timing tables

tSYNCH	200 ns	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tTRIG_MAX	250 ns	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held

5. Sample Applications

The Applications Manual contains many sample applications for use with Data Acquisition Processors. However, the DAP 5400a uses a different input configuration, which requires a different syntax for a few DAPL commands.

The most significant change to the DAPL syntax for the DAP 5400a is how inputs are configured. The DAP 5400a samples in groups, but after sampling is done, data can be selected and rearranged for transfer to the host PC. For example, if you are concerned with the inputs of only two channels, you do not need to send eight sampled channels to the PC.

In this chapter, two applications from the Applications Manual have been rewritten for the DAP 5400a. Following the syntax changes that were made in these examples, many examples in the Applications Manual can be modified for use with the DAP 5400a. Please note that analog output applications and digital input and output applications will not work with the DAP 5400a.

Example 1—Sampling Inputs Sequentially

This application configures the DAP 5400a to sample three input signals sequentially and send the digitized values to the PC. Since the DAP 5400a always samples input pins in groups, this application is different than for other Data Acquisition Processors where individual input pins are sampled (one from each group).

This application is similar to Application 1 in the Applications Manual. The IDEFINE, SET, and COPY commands have been changed for the DAP 5400a. The same single-ended input pins are used, but the differential input has been changed to single-ended input S8.

The following DAPL commands configure the Data Acquisition Processor for this application. Indentation is optional since DAPL ignores extra spaces.

```
RESET
IDEFINE A
  GROUPS 2
  SET IPIPES(0..7)  SPG1 //includes S1 connected to IP0 and
                         //S5 connected to IP2
  SET IPIPES(8..15) SPG0 //includes S8 connected to IP12
  TIME 100               //100 us between each group
END
PDEF B
  COPY(IPIPES(0,2,12),$BINOUT)
END
```

The RESET command on the first line clears all definitions and errors. It is a good idea to start each application with a RESET.

The next line begins an input procedure definition. An input procedure definition starts with the word IDEFINE and ends with the word END. IDEFINE often is abbreviated to IDEF. The IDEFINE command requires the name of the input procedure. "A" is the name chosen for the input procedure in this application.

The line GROUPS 2 configures the Data Acquisition Processor to sample two input channel groups, or 16 single-ended input pins. A unique feature of DAPL is its ability to assign logical processing channels to physical signals. The logical channel groups are associated with hardware pin groups. The pin groups can be sampled in any order in the logical channel sequence, and one set of signals can be sampled multiple times. After this logical association is defined, any individual channel can be processed independently as necessary.

The SET commands associate input channel groups with pin groups. Since inputs are connected to signal pins S1, S5, and S8, pin groups SPG1, and SPG0 must be used. The two SET commands connect input channel 0 (IP0) to single-ended input S1, input channel 2 (IP2) to single-ended input S5, and input channel 12 (IP12) to single-ended input S8.

The TIME command sets the sampling time to 100 microseconds. Since the input configuration samples two pin groups, each group is sampled every 200 microseconds.

END marks the end of the input procedure definition.

The word PDEFINE begins a processing procedure definition. PDEFINE is often abbreviated to PDEF. The PDEFINE command is followed by the name of the processing procedure, which is B in this application. You are free to choose other names for procedures in your applications.

The COPY command transfers binary data from input channels 0, 2, and 12 to the binary communications pipe $BINOUT. The Data Acquisition Processor transfers binary data through $BINOUT directly to the PC. The COPY task continues until sampling is stopped.

END marks the end of the processing procedure definition.

Data collection begins when a START command is issued:

```
START A, B
```

The COPY task transfers data values from each input channel pipe in order. The host program running on the PC must know the number of data channels sent from the Data Acquisition Processor in order to correctly display the data. Some programs automatically determine the number of data channels by examining the DAPL command file.

To stop sampling, issue a STOP command. This command stops the input procedure and the processing procedure. Analog sampling is stopped and the COPY task is halted. The application can be restarted by reissuing the START command.

This application can be simplified if the inputs are sampled simultaneously. To do this, all inputs must be from one pin group. Because there are only three channels to sample, the following example can use a four-channel sampling mode. The pin group SPG0 is used, which contains pins S0, S2, S4, and S6. Samples from S0, S2, and S4 are sent to the PC with the COPY command:

```
RESET
IDEFINE A
  GROUPSIZE 4
  GROUPS 1
  SET  IPIPES(0..3)  SPG0
  TIME 200
END
PDEF B
  COPY(IPIPES(0..2),$BINOUT)
END
```

Note that TIME was adjusted to make the data rate the same as with the first example.

After sampling, the three signals can be processed in any order. For example, we can rearrange the terms so they are transferred in the order S4, S0, S2, by listing the logical channels in a MERGE processing command.

```
PDEF B
  MERGE(IP2, IP0, IP1, $BINOUT)
END
```

Example 2—True Simultaneous Sampling

Some applications require sampling of two or more analog inputs simultaneously. The DAP 5400a can sample up to eight channels simultaneously. In this application, the DAP 5400a samples single-ended inputs S1, S3, S5, S7, S9, S11, S13, and S15 simultaneously, with all eight channels being sampled every 1000 microseconds.

This application is similar to Application 33 from the Applications Manual.

```
RESET
IDEFINE A
  GROUPSIZE 8
  GROUPS 1
  SET IPIPES(0..7) SPG1
  TIME 1000
END
```

All eight channels defined in the SET command will be sampled. Extra channels can be ignored if you do not need the data from all of the channels.

Example 3—Simulated Simultaneous Sampling

This application uses `FIRFILTER` commands to perform a time-shifting interpolation on 16 channels of raw data.

The DAP 5400a samples data in groups of eight channels. If all 16 analog inputs are sampled, the normal sampling sequence is to sample eight channels, then, one interval later, sample the next eight channels.

Sometimes it is necessary to get a "snapshot" of data, or to look at what is happening to all input data channels at one instant. This is known as simultaneous sampling. The DAP 5400a hardware is designed for simultaneous sampling of up to eight input channels. If more than eight channels are involved, a software correction to simulate simultaneous sampling is possible using the DSP features of the DAP 5400a hardware and software. In effect, the correction algorithms construct local approximating curves for each data sequence, and use the approximating curves to estimate the sample values that would have been recorded if all of the signals had been sampled at the same time. (Technically speaking, the approximating curves used in this application are the least-squares best fit of a cubic polynomial model.)

The approximation process has some drawbacks for the case of very high frequency signals because the approximation tends to suppress very rapid local changes in the data. However, if the rapid local changes are due to high frequency noise, the noise-suppression side effect is beneficial.

To create a software simulation of simultaneous sampling for sixteen channels, samples of both channel groups need to be taken in a repeating sequence.

The first eight channels do not need to be corrected, but this application applies filtering so that all 16 channels experience the same high-frequency noise reduction. The interpolation approximates the data in last eight channels for the time at which the first channel group was sampled by “time-shifting” the data in the second channel group by 1 sampling interval. Observe that data from each channel are processed independently.

The following DAPL commands configure the DAP 5400a for this application:

```
RESET
VECTOR SHIFT000 = (-3121, 4681, 9362, 10923, 9362, 4681,
  -3121)
VECTOR SHIFT050 = (-3700, 6845, 11160, 10825, 7418, 2517,
  -2298)
PIPES  P0, P1, P2, P3, P4, P5, P6, P7, P8, P9
PIPES  P10, P11, P12, P13, P14, P15
IDEF  SAMP
  GROUPS 2
  SET IP(0..7)   SPG0
  SET IP(8..15)  SPG1
  TIME  20.00
  END
PDEF  FILT
  FIRFILTER( IP0,  SHIFT000, 7, 1, 0, 0, P0 )
  FIRFILTER( IP1,  SHIFT000, 7, 1, 0, 0, P1 )
  FIRFILTER( IP2,  SHIFT000, 7, 1, 0, 0, P2 )
  FIRFILTER( IP3,  SHIFT000, 7, 1, 0, 0, P3 )
  FIRFILTER( IP4,  SHIFT000, 7, 1, 0, 0, P4 )
  FIRFILTER( IP5,  SHIFT000, 7, 1, 0, 0, P5 )
  FIRFILTER( IP6,  SHIFT000, 7, 1, 0, 0, P6 )
  FIRFILTER( IP7,  SHIFT000, 7, 1, 0, 0, P7 )
  FIRFILTER( IP8,  SHIFT050, 7, 1, 0, 0, P8 )
  FIRFILTER( IP9,  SHIFT050, 7, 1, 0, 0, P9 )
  FIRFILTER( IP10, SHIFT050, 7, 1, 0, 0, P10 )
  FIRFILTER( IP11, SHIFT050, 7, 1, 0, 0, P11 )
  FIRFILTER( IP12, SHIFT050, 7, 1, 0, 0, P12 )
  FIRFILTER( IP13, SHIFT050, 7, 1, 0, 0, P13 )
  FIRFILTER( IP14, SHIFT050, 7, 1, 0, 0, P14 )
  FIRFILTER( IP15, SHIFT050, 7, 1, 0, 0, P15 )
  MERGE( P0, P1, P2, P3, P4, P5, P6, P7, P8, P9, P10, \
         P11, P12, P13, P14, P15, $BINOUT )
END
START SAMP, FILT
```

The `RESET` command on the first line clears all definitions and errors.

The two `VECTOR` commands define data for two filters. `SHIFT000` is the filter data used for the first channel group and `SHIFT050` is the filter data used for the second channel group.

The `PIPES` commands define 16 data pipes for use by the `FIRFILTER` commands.

The input procedure SAMP configures input channel pipes 0-15 with the two input pin groups SPG0 and SPG1. This associates each analog input pin with one input channel pipe.

The TIME command sets the sampling interval to 20 microseconds. Since data is being time-corrected for two channel groups, the results will be an approximation for simultaneous sampling every 40 microseconds.

The processing procedure FILT is where the interpolation of data is configured. Each FIRFILTER command receives data from one input channel. Depending on which group the channel was sampled in, one of the two filter vectors is applied to the data. After the data are filtered, each sample is sent to a data pipe.

The MERGE command sends all filtered data to the PC through the binary communications pipe $BINOUT.

END marks the end of the processing procedure.

START begins processing of the input procedure SAMP and the processing procedure FILT. Sampling can be stopped by issuing a STOP command.

6. Appendix A: Analog Expansion Pin Mapping

Chapter 3 discussed how sampling of signals is always done in predetermined groups of size 4 of 8 depending on the configured sampling group size. This is also true when using MSXB 018 analog expansion boards, except that there are 64 signal lines rather than 16, so the signals are at different pin numbers on the expansion boards.

Expansion board MSXB 018 has four connectors J2 – J5 for analog input expansion. Each connector has 16 inputs numbered `S0` to `S15`, for a total of 64 analog inputs per board. The DAP 5400a can use up to eight analog input expansion boards, for a total of 512 analog inputs, or 64 pin groups. This Appendix documents how the expansion board pin numbers map to pin group numbers used in the DAPL `SET` commands.

Unlike other Data Acquisition Processors, the DAP 5400a has the same channel mapping with `OPTION AINEXPAND=ON` as it does with `OPTION AINEXPAND=OFF`. So `AINEXPAND` is not needed on the DAP 5400a.

For the DAP 5400a, all channel groups in an input procedure must be explicitly configured.

The mapping for one expansion board in 8-channel mode is:

MSXB 018 Expansion Mapping, 8-Channel Groups

Pin Group Name	MSXB 018 Pin Names (Connector)
SPG0	S0 (J5), S8 (J5), S0 (J4), S8 (J4), S0 (J3), S8 (J3), S0 (J2), S8 (J2)
SPG1	S1 (J5), S9 (J5), S1 (J4), S9 (J4), S1 (J3), S9 (J3), S1 (J2), S9 (J2)
SPG2	S2 (J5), S10 (J5), S2 (J4), S10 (J4), S2 (J3), S10 (J3), S2 (J2), S10 (J2)
SPG3	S3 (J5), S11 (J5), S3 (J4), S11 (J4), S3 (J3), S11 (J3), S3 (J2), S11 (J2)
SPG4	S4 (J5), S12 (J5), S4 (J4), S12 (J4), S4 (J3), S12 (J3), S4 (J2), S12 (J2)
SPG5	S5 (J5), S13 (J5), S5 (J4), S13 (J4), S5 (J3), S13 (J3), S5 (J2), S13 (J2)
SPG6	S6 (J5), S14 (J5), S6 (J4), S14 (J4), S6 (J3), S14 (J3), S6 (J2), S14 (J2)
SPG7	S7 (J5), S15 (J5), S7 (J4), S15 (J4), S7 (J3), S15 (J3), S7 (J2), S15 (J2)

Observe the following patterns in the pin assignments:
- For SPG0 the signal lines alternate S0, S8, S0, S8, etc.
- For SPG1 the signal lines alternate S1, S9, S1, S9, etc.
- Connector sequence is J5, J4, J3, J2.

The four-channel sampling mode is similar, except that predefined groups of four signals are sampled simultaneously. The mapping for one expansion board in 4-channel mode is:

MSXB 018 Expansion Mapping, 4-Channel Groups

Pin Group Name	MSXB 018 Pin Names (Connector)
SPG0	S0 (J5), S8 (J5), S0 (J4), S8 (J4)
SPG1	S1 (J5), S9 (J5), S1 (J4), S9 (J4)
SPG2	S0 (J3), S8 (J3), S0 (J2), S8 (J2)
SPG3	S1 (J3), S9 (J3), S1 (J2), S9 (J2)
SPG4	S2 (J5), S10 (J5), S2 (J4), S10 (J4)
SPG5	S3 (J5), S11 (J5), S3 (J4), S11 (J4)
SPG6	S2 (J3), S10 (J3), S2 (J2), S10 (J2)
SPG7	S3 (J3), S11 (J3), S3 (J2), S11 (J2)
SPG8	S4 (J5), S12 (J5), S4 (J4), S12 (J4)
SPG9	S5 (J5), S13 (J5), S5 (J4), S13 (J4)
SPG10	S4 (J3), S12 (J3), S4 (J2), S12 (J2)
SPG11	S5 (J3), S13 (J3), S5 (J2), S13 (J2)
SPG12	S6 (J5), S14 (J5), S6 (J4), S14 (J4)
SPG13	S7 (J5), S15 (J5), S7 (J4), S15 (J4)
SPG14	S6 (J3), S14 (J3), S6 (J2), S14 (J2)
SPG15	S7 (J3), S15 (J3), S7 (J2), S15 (J2)

The pin labels and connector names shown in this table correspond to the pin labels and connector names given in the MSXB 018 hardware manual.

Pin addresses on additional expansion boards are similar, but different ranges of pin group numbers select them.

Pin Group Ranges 8-channel Mode

```
SPG0 - SPG7 Expansion Board 0
SPG8 - SPG15 Expansion Board 1
                . . .
SPG56 - SPG63 Expansion Board 7
```

Pin Group Ranges 4-channel Mode

```
SPG0 - SPG15 Expansion Board 0
SPG16 - SPG31 Expansion Board 1
                . . .
SPG112 - SPG127 Expansion Board 7
```

To determine the conventional connector hardware pin numbers corresponding to the signal names on the expansion board, look in Table 1 of the MSXB 018 hardware manual.

7. Recalibration

Each Data Acquisition Processor is burned in and then calibrated by Microstar Laboratories as part of the manufacturing process. The accuracy of this calibration is sufficient for most applications. Accuracy is affected by three factors:

- The operating temperature of the Data Acquisition Processor
- Drift in the Data Acquisition Processor circuitry
- Analog voltage range selection.

The operating temperature is determined by a number of factors. If the Data Acquisition Processor is operated inside a personal computer, the operating temperature is affected by the number of expansion boards, power supply rating, fan efficiency, etc.

Component drift depends on total operating time of the unit as well as the number of times the unit has been powered up and down.

Changes to analog voltage ranges may require that the Data Acquisition Processor be recalibrated.

For applications requiring high accuracy, occasional recalibration may be necessary. For high absolute accuracy, the calibration sequence requires that measurements be made using at least a 5.5 digit digital voltmeter with a DC accuracy of 0.0015% (15 ppm) or better. In most applications, only relative accuracy is important, so recalibration with a less accurate digital voltmeter may be acceptable. The voltmeter is used to calibrate the precision on-board voltage reference. That reference then is used by the DAP 5400a, along with sampling the on-board ground, to self-calibrate offset and gain for each channel.

Since only the voltage reference is adjusted during the manual calibration procedure, calibration takes little time. The reference voltage is adjusted to 4.99329V with Trimmer A. The voltage reference is measured at header J6. Trimmer A and J6 are located in the upper left corner of the DAP5400a, between the two circuit boards. Calibration also is available from Microstar Laboratories for a nominal fee.

Index